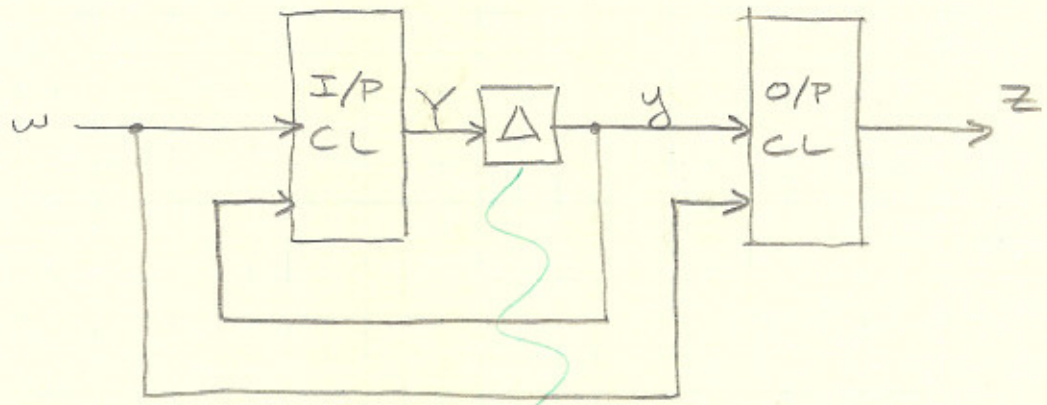
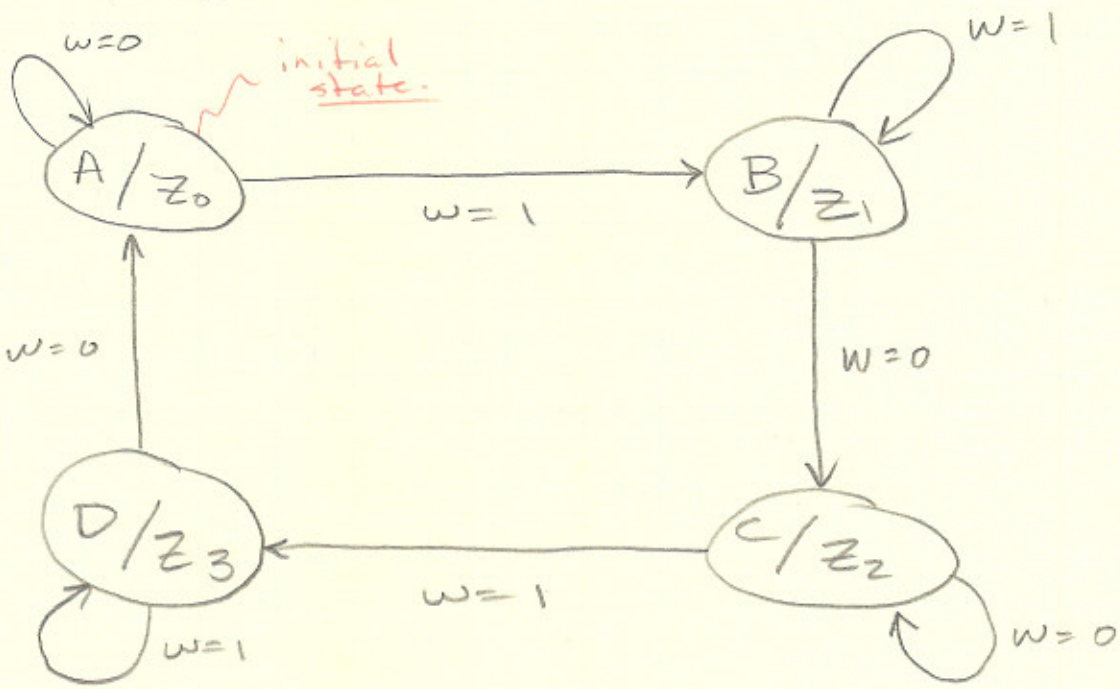
.... continued from last day.

Asynchronous Sequential Circuit



Δt time delay incoroporated into I/P_{CL}

State Diagram (1)



Flow table (2)

Current State	Next State w=1	Next State w=0	Output
A	B	A	Z_0
B	B	C	Z_1
C	D	C	Z_2
D	D	A	Z_3

State Assignment (3)

State	y_1	y_0
A	0	0
B	0	1
C	1	1
D	1	0

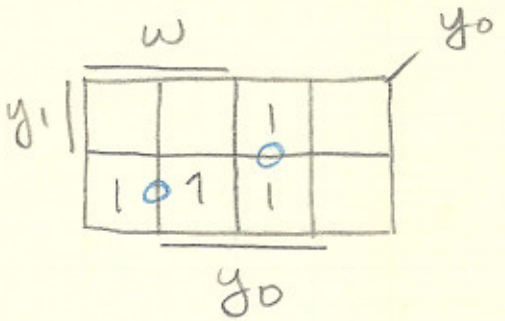
only one bit should change here, as well.

Note: Only one bit may change when changing states

State Assignment Table (4)

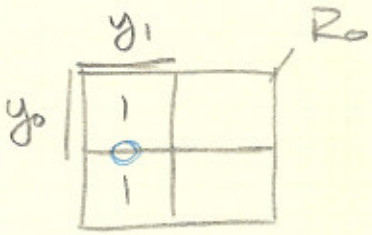
Current State y_1	Current State y_0	Next State w=1 y_1	Next State w=1 y_0	Next State w=0 y_1	Next State w=0 y_0	Output R_1	Output R_0
0	0	0	1	0	0	1	0
0	1	0	1	1	1	0	0
1	1	1	0	1	1	1	1
1	0	1	0	0	0	0	1

Functions (5)



$$Y_0 = \bar{w}\, y_0 + \bar{y}_1\, w$$

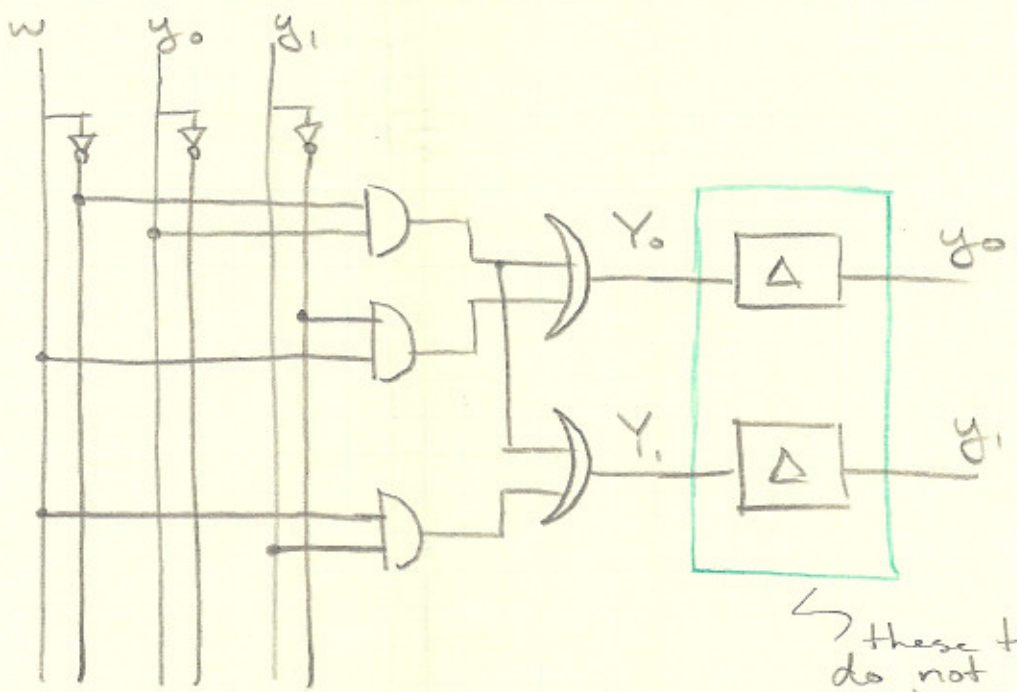
Likewise... perform operation for y_1



$$R_0 = y_1$$

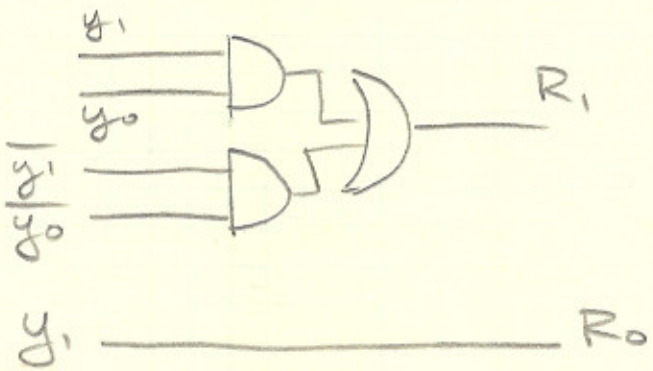
Likewise... perform operation for ~~R_1~~

Circuit

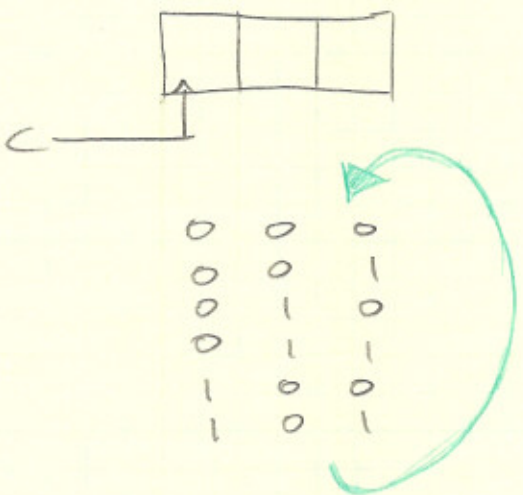


these time delays do not need to be included b/c they are included in the logic circuit.

The other half of the circuit



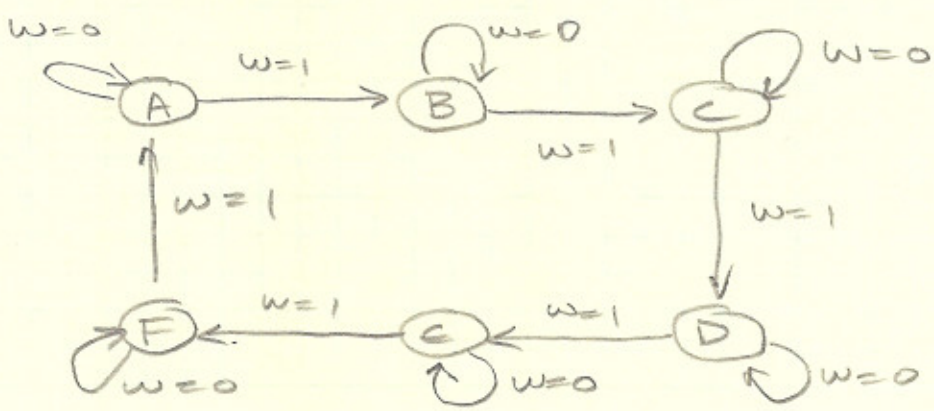
Digital System Design



0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1

Skip over the last two states.

This results in the following state diagram



Z	R_2	R_1	R_0
Z_0	0	0	0
Z_1	0	0	1
Z_2	0	1	0
Z_3	0	1	1
Z_4	1	0	0
Z_5	1	0	1

For HW; design the synchronous Sequential Circuit using D Latches.